REMARKS

Items 1 -5 in the office action require a substitute specification including claims and a substitute abstract.

In response, the applicant submits with this amendment a substitute specification including claims and abstract. The substitute specification reformats the original specification, adds to the specification the cross-reference to the priority provisional application, and adds to the specification a statement as to federally sponsored research. No new matter has been added.

Items 6-8 in the office action reject all claims under the second paragraph of 35 USC 112 as indefinite, noting exemplary defects in a number of claims.

In response, the undersigned has carefully reviewed the claims and amended all claims to avoid ambiguity and indefiniteness.

Items 9-10 in the office action reject claims 27-35 under 35 USC 102(e) as anticipated by United States patent 5,945,718 to Passlack et al.

In response, the applicant cancels claims 27-35.

Dependent claim 36 has been placed in independent form in order to avoid the rejection of base claim 34 from which it depended.

Dependent claim 37 has been amended to delete its dependence on rejected claim 33.

New claim 38 has been added by combining the limitations of claim 37 and 33 into an independent claim in order to overcome the rejection of claim 37 as to claim 33.

New claims 38 to 54 more broadly claim the novel gate structure.

The rapid thermal annealing and 700 to 900 degree temperature range now claims are disclosed in the substitute specification in the paragraph spanning pages 8 and 9.

In view of the foregoing comments, the applicant believes this application is in condition for allowance, and allowance is now requested.

If Examiner Kang wishes to make an examiner's amendment in order to overcome some minor matter in order to more promptly allow this application he should telephone the undersigned to request authorization.

Respectfully Submitted,

4/22/02
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MARKED UP COPY OF THE CLAIMS

1. (Amended) An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure comprising a first layer and a second layer;

[a layer composed of the] said first layer substantially comprising compounds of gallium and oxygen [including but not limited to mixtures of Ga_2O_3, Ga_2O and other gallium oxygen compounds positioned on upper surface of said compound semiconductor wafer structure];

[a second insulating] said second layer [composed of the] comprising compounds of gallium and oxygen and at least one [or more] rare earth element[s layer that form an insulating layer deposited on top of the initial supporting gallium oxygen layer, with said first and second layers forming a gate insulator structure adjacent to and on top of the compound semiconductor structure];

a [stable refractory metal] gate electrode positioned on [upper surface of] said gate insulator structure [layers];

source and drain ion implants self-aligned to [the] said gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;

wherein [the refractory metal] gate electrode comprises a [refractory] metal selected from the group consisting of W, WN_x [or] WSi_x [or] and combinations thereof[;

means of interconnection of said transistors forming a monolithically integrated circuit].

2. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1] The transistor of claim 1 wherein [the initial layer of gallium oxygen compounds] said first layer forms an atomically abrupt interface with [the] said upper surface [of the compound semiconductor wafer structure].

3. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1] The transistor of claim 1 wherein [the] said gate insulator structure is composed of at least three layers, [an initial gallium oxygen compound layer, a graded layer that contains varying compositions of gallium oxygen and at least one rare-earth element, and a third insulator layer that is composes largely of a compound of gallium, oxygen and one or more rare earth elements and] including a graded layer that contains varying compositions of gallium oxygen and at least one rare-earth element.

4. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1] The transistor of claim 3 wherein [the] said gate insulator structure [is composed of more than three multiple layers, an initial gallium oxygen compound layer, and multiple layers] further comprises at a third layer containing gallium and oxygen [with or without the inclusion of one or more rare earth elements that together form an insulating gallium oxide gate insulator structure].

5. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1] The transistor of claim 1 wherein [the initial gallium

oxygen compound layer] said first layer has a thickness of more than 10 angstroms and less than 25 angstroms.

6. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1] The transistor of claim 1 wherein [the] said gate insulator structure has [an overall] a [total] thickness of 20-300 angstroms.

7. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1] The transistor of claim 1 wherein [the initial gallium oxygen compound] said first layer forms an [atomically abrupt] interface with [the compound semiconductor structure] said upper surface that extend less than four atomic layers in depth of structural interface modulation.

8. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1] The transistor of claim 1 wherein [the initial gallium and oxygen compound] said first layer and [the] said gate insulator structure protects [the] said upper surface [of the compound semiconductor wafer structure].

9. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1] The transistor of claim 1 wherein [the refractory metal] said gate electrode comprises a refractory metal which is stable in presence of the top layer of the gate insulator structure at [an elevated temperature of] 700°C [and above].

10. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1] The transistor of claim 1 wherein [the] said source and drain ion implants [comprising said enhancement mode metal-oxide-compound semiconductor field effect transistor being an] provide one of an n-channel [device] or p-channel [device].

11. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1] The transistor of claim 1 wherein [the] said source and drain ion implants comprise [and] at least one of Be/F [or] and C/F[, said enhancement mode metal-oxide-compound semiconductor field effect] transistor being a p-channel device].

12. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1] The transistor of claim 1 wherein [the] said upper surface [of the compound semiconductor wafer structure] comprises GaAs.

13. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1] The transistor of claim 1 wherein [the] said upper surface [of the compound semiconductor wafer structure] comprises $In_xGa_{1-x}As$.

14. (Amended) An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

gate insulator structure on said upper surface, said gate insulator structure comprising a first layer, a second layer, and a third layer;

[a layer composed of the] said first layer substantially comprising compounds of gallium and oxygen [compounds including but not limited to mixtures of Ga_2O_3, Ga_2O and other gallium oxygen compounds positioned on upper surface of said compound semiconductor wafer structure];

[a second insulating layer deposited upon the] said second layer [first layer and composed of the] substantially comprising compounds of gallium and oxygen and at least one

[or more] rare earth element[s] such that the normalized relative composition of at least one of gallium, oxygen, and [one or more] said at least one rare earth element[s] in said second layer [are changing] varies in a monotonic manner as a function of [the thickness] depth within said second insulating layer;

[a third insulating] said third layer [deposited on top of] above said second layer, said third layer substantially comprising [composed of] gallium oxygen and at least one [or more] rare earth element[s], said third layer being insulating, [wherein said first, second, and third layers form a gate insulator structure adjacent to and deposited on top of the compound semiconductor structure];

a [stable refractory metal] gate electrode positioned on [upper surface of] said gate insulator structure [layers];

source and drain ion implants self-aligned to [the] said gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;

wherein [the refractory metal] said gate electrode comprises a [refractory] metal selected from the group consisting of W, WN, [or] WSi , and [or] combinations thereof[;

means of interconnection of said transistors forming a monolithic integrated circuit].

15. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14] The transistor of claim 14 wherein [the initial layer of gallium oxygen compounds] said first layer forms an atomically abrupt interface with [the] said upper surface [of the compound semiconductor wafer structure].

16. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14] The transistor of claim 14 wherein the gate insulator structure [is composed of three or more layers, an initial gallium oxygen compound layer, a graded layer that contains varying compositions of] comprises a varying layer that substantially comprises gallium, oxygen, and at least one rare-earth element in which relative concentration of at least one of gallium, oxygen, and said at least one rare earth in said varying layer monotonically vary with depth in said layer, [and a third insulator layer that is composes largely of a compound of gallium, oxygen and one or more rare earth elements].

17. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14] The transistor of claim 14 wherein [the initial gallium oxygen compound] said first layer has a thickness of more than 10 angstroms and less than 25 angstroms.

18. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14] The transistor of claim 14 wherein the gate insulator structure has [an overall total] a thickness of 20-300 angstroms.

19. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14] The transistor of claim 14 wherein [the initial gallium oxygen compound] said first layer forms an [atomically abrupt] interface with the compound semiconductor wafer structure that extend less than four atomic layers in depth of modulation of said interface.

20. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14] The transistor of claim 14 wherein [the initial gallium

and oxygen compound] said first layer and [the] said gate insulator structure protects [the] said upper surface [of the compound semiconductor wafer structure].

21. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14] The transistor of claim 14 wherein [the refractory metal] said gate electrode comprises a [refractory] metal which is stable in presence of the top layer of the gate insulator structure at [an elevated temperature of] 700°C [and above].

22. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14] The transistor of claim 14 wherein [the] said source and drain ion implants [comprising said enhancement mode metal-oxide-compound semiconductor field effect transistor being] define an n-channel [device].

23. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14] The transistor of claim 14 wherein [the] said source and drain ion implants comprise and Be/F and C/F, [said enhancement mode metal-oxide-compound semiconductor field effect transistor being a] and define a p-channel [device].

24. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14] The transistor of claim 14 wherein [the] said upper surface [of the compound semiconductor wafer structure] comprises GaAs.

25. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14] The transistor of claim 14 wherein [the] said upper surface [of the compound semiconductor wafer structure] comprises $In_xGa_{1-x}As$.

26. An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a multilayer gate insulator structure [composed of] positioned on said upper surface, said multilayer gate insulator structure substantially comprising alternating layers each of which comprises [comprised of] gallium, oxygen, and at least one rare-earth element [forming a gate insulator with low electronic midgap defect density positioned on upper surface of said compound semiconductor wafer structure];

a [stable refractory metal] gate electrode positioned on [upper surface of] said multilayer gate insulator structure [layer];

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;[,]

[wherein] and dielectric spacers [are] positioned on sidewalls of [the stable refractory gate metal] said gate electrode.

27-35. - Canceled by this amendment.

36. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 34] An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure positioned on upper surface of said compound semiconductor wafer structure;

a [stable refractory metal] gate electrode positioned on upper surface of said gate insulator structure layer;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas[,];

wherein [the] said compound semiconductor wafer structure comprises a Al_xGa_{1-x} As, $In_yGa_{1-y}As$, InP, or $In_zGa_{1-z}P$ layer, said layer being positioned on said upper surface [of a compound semiconductor substrate];

a substrate on which resides said compound semiconductor wafer structure; and

wherein [the compound semiconductor] said substrate includes a InP based semiconductor wafer.

37. (Amended) [An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1, 13, 26, and 33] A complementary metal-oxide compound semiconductor integrated circuit comprising the transistor of claim 1, 13, or 26 [that may be] integrated together with similar and complementary transistor devices to form said complementary metal-oxide compound semiconductor integrated circuit[s].

NEW CLAIMS

Claim 38 is modeled after claim 37/33.

38. A complementary metal-oxide compound semiconductor integrated circuit comprising an enhancement mode metal-oxide-compound semiconductor field effect transistor, said transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure positioned on said upper surface;

a gate electrode positioned on said upper surface;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas,

wherein the compound semiconductor wafer structure comprises a wider band gap spacer layer and a narrower band gap channel layer;

wherein the narrower band gap channel layer comprises $In_yGa_{1-y}As$; and

and wherein said transistor is integrated together with similar and complementary transistor devices to form complementary metal-oxide compound semiconductor integrated circuit.

Claim 39 is modeled after claim 1.

39. An enhancement mode metal-oxide-compound semiconductor field effect transistor structure, comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure comprising a first layer and a second layer, said gate insulator on said upper surface;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer comprising at least one compound of gallium, oxygen and at least one rare earth element; and

a gate electrode positioned on said gate insulator structure.

40. The structure of claim 39 wherein said gate electrode comprises a refractory metal.

41. The structure of claim 39 wherein said gate electrode comprises a member of the group consisting of W, WN_x, WSi , and combinations thereof.

42. The structure of claim 39 wherein said gate insulator structure further comprises a third layer.

43. The structure of claim 42 wherein said third layer comprises compounds comprising gallium and oxygen.

44. The structure of claim 43 wherein compounds of said third layer comprising gallium and oxygen further comprise a rare earth element.

45. The structure of claim 44 wherein a composition of said third layer varies monotonically with depth in said third layer.

46. The structure of claim 43 wherein said gate insulator structure further comprises a fourth layer.

47. The structure of claim 43 wherein said fourth layer comprises compounds comprising gallium and oxygen.

48. The structure of claim 47 wherein compounds of said fourth layer comprising gallium and oxygen further comprise a rare earth element.

49. The structure of claim 39 wherein said first layer is adjacent and in contact with said upper surface.

50. The structure of claim 39 further comprising source and drain contacts.

51. The structure of claim 39 wherein said source and drain contacts are rapid thermal annealed in UHV.

52. The structure of claim 39 wherein said gate insulator structure passivates said upper surface.

53. A method for forming an enhancement mode metal-oxide-compound semiconductor field effect transistor structure, comprising:

providing a compound semiconductor wafer structure having an upper surface;

depositing a gate insulator structure comprising depositing a first layer and depositing a second layer, said gate insulator on said upper surface;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer comprising at least one compound of gallium, oxygen and at least one rare earth element; and

depositing a gate electrode positioned on said gate insulator structure.

54. The method of claim 53 comprising rapid thermal annealing said structure in UHV.

55. The method of claim 54 wherein said rapid thermal annealing comprising annealing at between 700 and 900 degrees Centigrade.

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